"Method and Apparatus to Improve Memory Performance"
by Jonathan C. Lueker, et al.
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**FIG.1**



**FIG.2**

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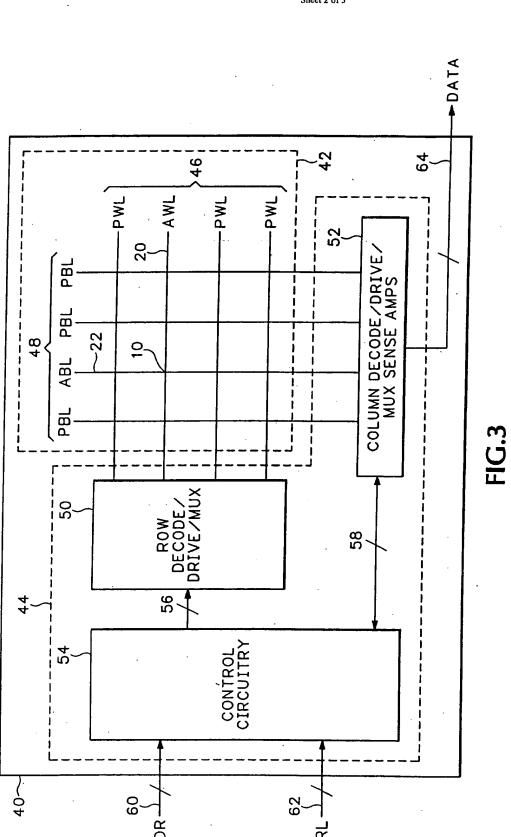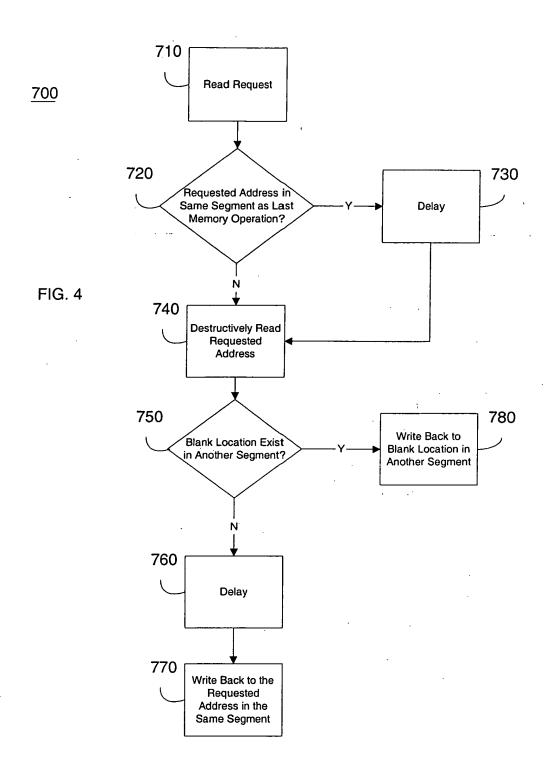Contact: Anthony M. Martinez @ (480) 552-0624, Reg. No.: 44,223
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FIG.3

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700

710

Read Request

720

Requested Address in Same Segment as Last Memory Operation?

— Y → 730

Delay

N

740

Destructively Read Requested Address

750

Blank Location Exist in Another Segment?

— Y — 780

Write Back to Blank Location in Another Segment

N

760

Delay

770

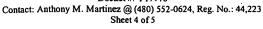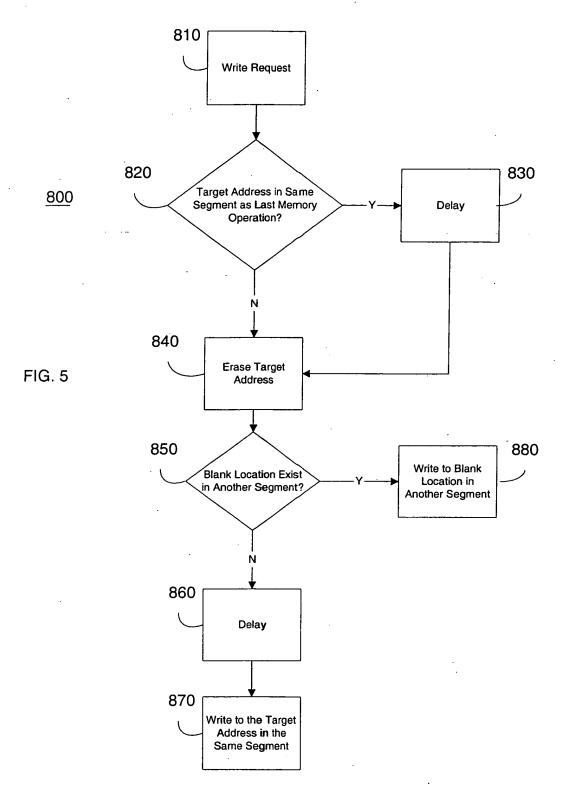Write Back to the Requested Address in the Same Segment

FIG. 4

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FIG. 5

810 Write Request

800

820 Target Address in Same Segment as Last Memory Operation?

—Y→ 830 Delay

N

840 Erase Target Address

850 Blank Location Exist in Another Segment?

—Y→ 880 Write to Blank Location in Another Segment

N

860 Delay

870 Write to the Target Address in the Same Segment

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FIG. 6

900

910 — PROCESSOR

920 — MEMORY CONTROLLER

940 — MASS STORAGE

930 — CACHE MEMORY